The Patent Office

SN 680,747

The Patent Office
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NP9 1RH

I, the undersigned, being an officer duly authorised in accordance with Section 62(3) of the Patents and Designs Act 1907, to sign and issue certificates on behalf of the Comptroller-General hereby certify that annexed hereto is a true copy of the documents as originally filed in connection with the Patent application identified therein.

In accordance with the Patents (Companies Re-registration) Rules 1982, if a company named in this certificate and any accompanying documents has re-registered under the Companies Act 1980 with the same name as that with which it was registered immediately before re-registration save for the substitution as, or the inclusion as, the last part of the name of the words "public limited company" or their equivalents in Welsh, references to the name of the company in this certificate and any accompanying documents shall be treated as references to the name with which it is so re-registered.

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Witness my hand this
23rd day of APRIL 1991

W. Russell

PATENTS ACT 19

PATENTS FORM NO. 1/77 (Revised 1982)

(Rules 16, 19)

The Comptroller
The Patent Office

- 6 APR 1990

-9APR'90#001A2946 PAT 1 77 UC 15.00

REQUEST FOR GRANT OF A PATENT

9007789.2

THE GRANT OF A PATENT IS REQUESTED BY THE UNDERSIGNED ON THE BASIS OF THE PRESENT APPLICATION

I Applicant's or Agent's reference *(Please insert if available)* P/2224(155)

II Title of invention Method for dram sensing current control

III Applicant or Applicants *(See note 2)*

Name (First or only applicant) RICHARD C. FOSS

Country Canada State Ontario ADP Code No. 38667790001

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(for the three other ~~inventors~~ Applicants please see attached sheet)

IV Inventor (see note 3)

(a) The applicant(s) ~~is~~/are the ~~sole~~/joint inventor(s)

or

~~(b) A statement on Patents Form No 7/77 is/will be furnished~~

V Name of Agent (if any) *(See note 4)* T.Z. GOLD & COMPANY ~~Chartered Patent Agents~~ ADP CODE NO 75618900 1

VI Address for Service *(See note 5)*
9, Staple Inn,
London, WC1V 7QH (Telephone 01 242 5240)

VII Declaration of Priority *(See note 6)*

Country	Filing date	File number

THE PATENT OFFICE
- 6 APR 1990
STATIONERS HALL
COURT LONDON

VIII The Application claims an earlier date under Section 8(3), 12(6), 15(4), or 37(4) *(See note 7)*

Earlier application or patent number ..... and filing date .....

TSAF 0301

IX Check List *(To be filled in by applicant or agent)*

A The application contains the following number of sheet(s)

1 Request ..... One ..... Sheet(s)

2 Description ... 2 ..... Sheet(s)

3 Claim(s) ..... Nil ..... Sheet(s)

4 Drawing(s) ..... One ..... Sheet(s)

5 Abstract ..... Nil ..... Sheet(s)

B The application as filed is accompanied by:-

1 Priority document . No

Translation of priority document No

3 Request for Search ... No .....

4 Statement of Inventorship and Right to Grant .... No .....

X It is suggested that Figure No.....of the drawings (if any) should accompany the abstract when published.

XI Signature *(See note 8)* Pusey

T.Z. GOLD & COMPANY, Agents for the Applicants

NOTES:

1. This form, when completed, should be brought or sent to the Patent Office together with the prescribed fee and two copies of the description of the invention, and of any drawings. 1+1

2. Enter the name and address of each applicant. Names of individuals should be indicated in full and the surname or family name should be underlined. The names of all partners in a firm must be given in full. Bodies corporate should be designated by their corporate name and the country of incorporation and, where appropriate, the state of incorporation within that country should be entered where provided. Full corporate details, eg a "corporation organised and existing under the laws of the State of Delaware, United States of America", trading styles, eg "trading as xyz company", nationality, and former names, eg "formerly (known as) ABC Ltd" are *not* required and should *not* be given. Also enter applicant(s) ADP Code No.(if known).

3. Where the applicant or applicants is/are the sole inventor or the joint inventors, the declaration (a) to that effect at IV should be completed, and the alternative statement (b) deleted. If, however, this is not the case the declaration (a) should be struck out and a statement will then be required to be filed upon Patent Form No 7/77.

4. If the applicant has appointed an agent to act on his behalf, the agent's name and the address of his place of business should be indicated in the spaces available at V and VI. Also insert agent's ADP Code No. (if known) in the box provided.

5. An address for service in the United Kingdom to which all documents may be sent must be stated at VI. It is recommended that a telephone number be provided if an agent is not appointed.

6. The declaration of priority at VII should state the date of the previous filing and the country in which it was made and indicate the file number, if available.

7. When an application is made by virtue of section 8(3), 12(6), 15(4) the appropriate section should be identified at VIII and the number of the earlier application or any patent granted thereon identified.

8. Attention is directed to rules 90 and 106 of the Patent Rules 1982.

9. Attention of applicants is drawn to the desirability of avoiding publication of inventions relating to any article, material or device intended or adapted for use in war (Official Secrets Acts, 1911 and 1920). In addition after an application for a patent has been filed at the Patent Office the comptroller will consider whether publication or communication of the invention should be prohibited or restricted under section 22 of the Act and will inform the applicant if such prohibition is necessary.

10. Applicants resident in the United Kingdom are also reminded that, under the provisions of section 23 applications may not be filed abroad without written permission or unless an application has been filed not less than six weeks previously in the United Kingdom for a patent for the same invention and no direction prohibiting publication or communication has been given or any such direction has been received.

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Method for DRAM Sensing Current Control

Peak sensing current in high speed DRAM must be controlled to prevent excessive resistive and inductive voltage drops in power supply connections. Two methods which can be used alone or in combination are described. The first isolates the bitline capacitance from the sense-amp to allow faster sensing. The second provides local sense clock drivers tailored for peak current control.

A typical CMOS DRAM sense amplifier is shown in fig.5.1. Speed is limited by two factors in this topology. The sense amplifier is connected directly to the bitlines, which typically have a capacitance around 0.5pF. Most of the current during sensing is consumed in charging these capacitors. Before data can be read onto the data bus a BL-BL* differential exceeding a certain noise margin must be attained, hence the bit line capacitance limits memory access time.

Another problem in large memory arrays is the voltage drop in sense and restore clock lines. One approach in controlling sensing current is to use slow sense and restore clock drivers to turn on sense amplifiers gradually. This is difficult to achieve uniformly for all sense amplifiers in a large array. Resistive drops in the connection from driver to the far end of the array mean that the near devices experience hard sensing while the far ones are very slow. Memory access must wait for the slowest column.

Bit line isolation devices isolate the sense node from the bitlines during the initial sensing period to allow a large voltage differential to develop quickly on the sense nodes and enable fast y-access turn-on. Earlier implementations of bitline isolation featured gate control which completely turned off the devices between the time the memory cell capacitor dumped charge onto the bit line and sensing started. Not only is it dangerous to use only a fraction of total charge differential for sensing, but speed is sacrificed to add an additional step in a memory access sequence.

FIG. 5.2,

The new technique uses an n-channel isolation device with gate held normally at a boosted Vpp supply falling to Vdd during the first part of sensing, and/or a p-channel device normally biased at the negative Vbb supply brought up to Vss during sensing. With typical DRAM processing both devices have thresholds of about 2v due to body

effect. Even in the high resistance state they allow memory cell capacitor charge to flow onto the sense node. Timing of the low impedance to high impedance transition is therefore not critical. During sensing they limit bitline voltage to Vdd-Vtn or Vss+Vtp and allow the sense node voltage differential to develop faster. The use of Vbb and Vpp supplies which already exist for other purposes on a high speed DRAM means that this technique does not require a substantial increase in complexity. In fact the additional capacitive load of isolation devices in inactive arrays creates a useful Vpp reservoir capacitor.

A second method of controlling sensing current is to use local phi-S pulldowns and/or local phi-R pullups. The pulldowns may be shared among several columns. The sense clocks which are routed the length of the array have less skew from near to far end because the load is greatly reduced. The slope of these clocks can be uniformly controlled to regulate sensing current.

The two methods of sensing current control can be utilized alone or in combination. For example, n-channel isolation devices could be used in conjunction with local phi-S pulldowns to control peak Vdd current and Vss current respectively.

Advantages

1. Speed - faster sensing because sense node voltage differential develops faster for the same sense current power budget.
2. No additional timing constraints.
3. Large Vdd and Vss power tracks are routed through the array instead of large sense clock tracks. The wide power bussing can be used elsewhere.
4. Reliability - leaky columns which have been de-programmed will not drag down the sense clocks if local sense clock drivers are shared only among columns with the same redundancy address.
5. Shared Circuitry - Vbb and Vpp supplies needed for isolation devices already exist on chip.
6. Isolation devices are used in combination with V_{pp} for W/L use Vss power bussing is achieved in combination with end-to-end architectures. The use of W/L Vss clamps at both ends, so that quiet W/L's serve as Vss bus/ground, plane could be linked.

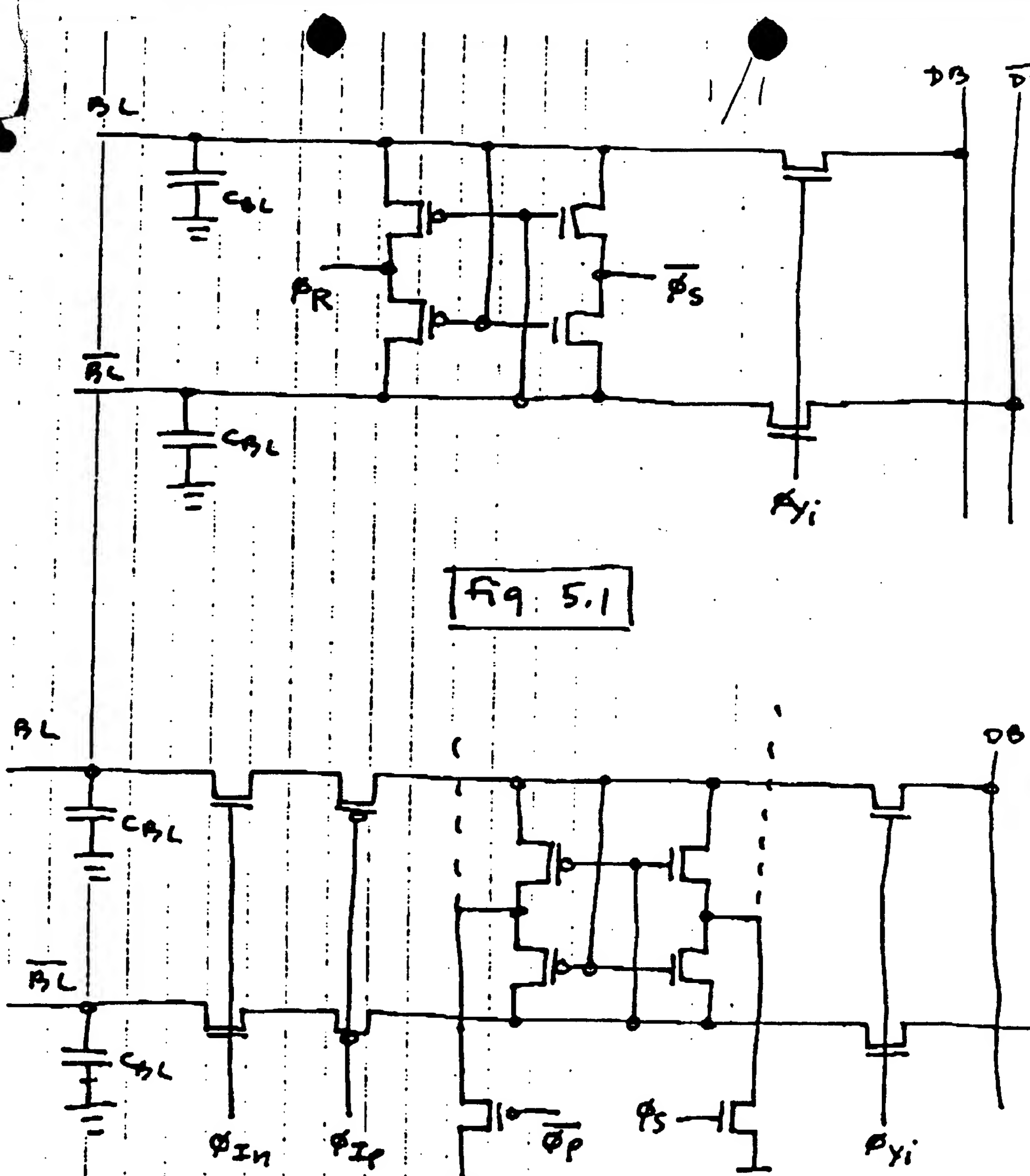
BL
C_{BL}
ϕ_R
$\overline{BL}$
C_{BL}
$\overline{\phi_S}$
DB
$\overline{DB}$
ϕ_{Yi}

Fig 5.1

BL
C_{BL}
$\overline{BL}$
C_{BL}
ϕ_{In}
ϕ_{Ip}
$\overline{\phi_P}$
V_{DD}
ϕ_S
ϕ_{Yi}
DB
$\overline{DB}$
W/L
V_{PP}
ϕ_{In}
V_{PP}
ϕ_{Ip}
V_{SS}
V_{BB}
ϕ_S
$\overline{\phi_P}$

fig 5.2

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e-registration under the Companies Act does not constitute new legal entity but merely subjects the company to rtain additional company law rules.

Witness my hand this
13th day of MAY 1991

W. Lunell

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